LDO Regulators with Watch-Dog Timer

500mA Output LDO Regulators with Voltage Detector and Watchdog Timer

BD3020HFP BD3021HFP

General Description

BD3020HFP BD3021HFP is a regulator IC with integrated WDT (Watch Dog Timer), high output voltage accuracy ±2.0 % and 80 μA (Typ) low circuit current consumption. These are supports usage of low ESR ceramic capacitor for output stability. The reset detection voltage can be adjusted by connecting resistors on the Vs terminal (BD3020HFP). They can be a stable power supply for any applications while detecting malfunction of microcontrollers.

Features

- Integrated WDT Reset Circuit
  [BD3020HFP]: Adjustable Detection Voltage through Vs pin
  [BD3021HFP]: WDT Can be Switched ON / OFF by Using INH Pin
- Low saturation voltage by using PMOS output transistor
- VCC Max Voltage: 50 V
- Integrated Over Current Protection and Thermal Shut Down
- HRP7 package

Key specification

Low Circuit Current:	80 μA (Typ)
Output Voltage:	5.0 V (Typ)
Output Current:	500 mA
High Output Voltage Accuracy:	±2 %
Low ESR ceramic capacitor can be used as output capacitor	

Package

W (Typ) × D (Typ) × H (Max)

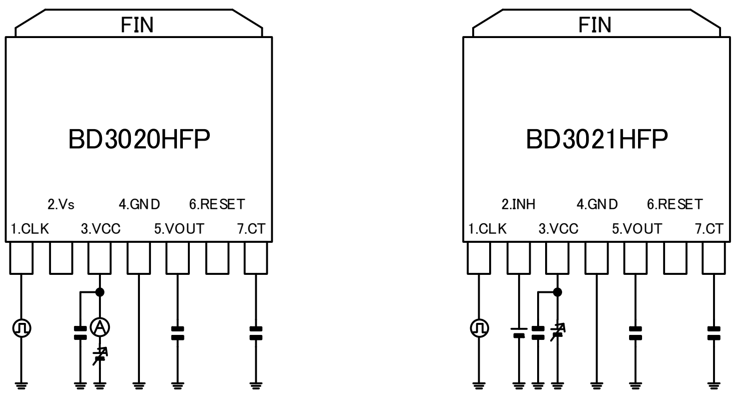
- HRP7 9.395 mm × 10.540 mm × 2.005 mm

Figure 1. Package Outlook

Applications

- Automotive (body, audio system, navigation system, etc.)

Typical Application Circuits



BD3020HFP BD3021HFP

Figure 2. Typical Application Circuits

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Ordering Information

B	D	3	0	2	X	H	F	P	-	T	R

Part number
3020
3021

Package
HFP: HRP7

Taping
TR: reel-wound embossed tamping

Pin Configuration

(TOP VIEW)

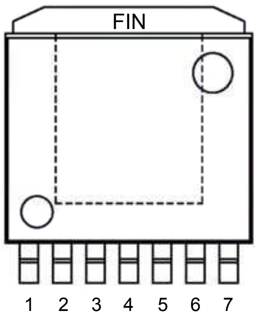


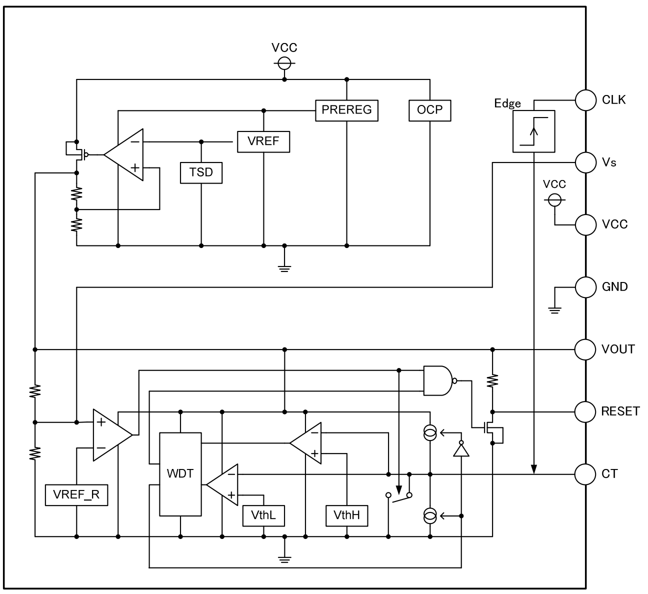
Figure 3. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	CLK	Clock Input from Microcontroller
2	Vs (BD3020HFP)	Reset Detection Voltage Set Pin
	INH (BD3021HFP)	WDT ON/OFF Function Pin
3	VCC	Power Supply Pin
4	GND	GND
5	VOUT	Voltage Output Pin
6	RESET	Reset Output Pin
7	CT	External Capacitance for Reset Output Delay Time, WDT Monitor Time Setting Connection Pin
Fin	GND	GND

Block Diagram

<BD3020HFP>



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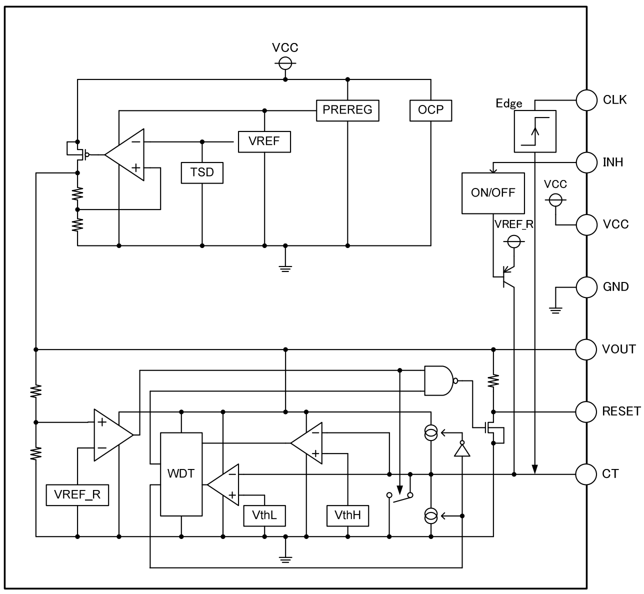


Figure 4. Block Diagrams

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply Voltage (1)	V_{CC}	-0.3 to +50.0	V
Vs pin Voltage (BD3020HFP)	Vs	-0.3 to +15.0	V
INH pin Voltage (BD3021HFP)	V_{INH}	-0.3 to +15.0	V
Regulator Output pin Voltage	V_{OUT}	-0.3 to +15.0	V
Reset Output pin Voltage	V_{RESET}	-0.3 to +15.0	V
Watchdog Input pin Voltage	V_{CLK}	-0.3 to +15.0	V
Reset Delay Setting pin Voltage	V_{CT}	-0.3 to +15.0	V
Power Dissipation (2)	Pd	1.6	W
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(1) Pd should not be exceeded.
(2) HRP7 mounted on 70.0 mm × 70.0 mm × 1.6 mmt Glass-Epoxy PCB. If Ta ≥ 25 °C, reduce by 12.8 mW / °C.
(1-layer PCB: Copper foil area on the reverse side of PCB: 0 mm × 0 mm)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Operating Conditions (-40°C ≤ Ta ≤ +125 °C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (3)	V_{CC}	5.6	36.0	V
Output Current	Io	0	500	mA

(3) For the output voltage, consider the voltage drop (dropout voltage) due to the output current.

Electrical Characteristics (Unless otherwise specified, -40°C ≤ Ta ≤ +125 °C, V_{CC} = 13.5 V, V_{CLK} = GND)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Overall Device						
Bias Current 1	Icc1	–	80	130	μA	Io = 0 mA
Bias Current 2	Icc2	–	150	300	μA	Io = 50 mA (Ta = 25 °C)
Regulator						
Output Voltage	V_{OUT}	4.90	5.00	5.10	V	Io = 200 mA
Line Regulation	Line.Reg	–	5	35	mV	5.6 V ≤ V_{CC} ≤ 36 V
Load Regulation	Load.Reg	–	30	70	mV	5 mA ≤ Io ≤ 200 mA
Dropout Voltage	ΔVd	–	0.3	0.6	V	V_{CC} = 4.75 V, Io = 200 mA
Ripple Rejection	R.R.	45	55	–	dB	f = 120Hz, ein = 1 Vrms, Io = 100 mA
Reset						
Detection Voltage (BD3020HFP)	Vdet	4.02	4.10	4.18	V	
Detection Voltage (BD3021HFP)	Vdet	4.40	4.50	4.60	V	
Hysteresis Width	V_{HS}	50	100	150	mV	
Output Delay Time Low→High (Power On Reset Time)	t_{dLH}	1.1	1.9	2.7	ms	V_{CC} = Vdet ±0.5 V (V_{CC} = V_{OUT}) INH = open(1), C_{CT} = 0.01 μF
Output Delay Time High→Low	t_{dHL}	–	100	300	μs	V_{CC} = Vdet ±0.5 V (V_{CC} = V_{OUT}) INH = open(1), C_{CT} = 0.01 μF
RESET Discharge Current	I_{RESET}	0.2	–	–	mA	V_{CC} = 1.5 V, V_{RESET} = 0.5 V (V_{CC} = V_{OUT})
CT Discharge Current	Ict	0.1	–	–	mA	V_{CC} = 1.5 V, V_{CT} = 0.5 V (V_{CC} = V_{OUT})
Low Output Voltage	V_{RST}	–	0.1	0.2	V	V_{OUT} = 4.0 V
Min Operating Voltage	V_{OPL}	1.5	–	–	V	

(1) BD3021HFP only

Electrical Characteristics (Unless otherwise specified, -40°C, ≤ Ta ≤ +125 °C, V_{CC} = 13.5 V, V_{CLK} = GND)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Watchdog timer						
CT Switching Threshold Voltage High	VthH	1.08	1.15	1.25	V	WDT ON(1), INH = open(1)
CT Switching Threshold Voltage Low	VthL	0.13	0.15	0.17	V	WDT ON(1), INH = open(1)
WDT Charge Current	Ictc	3.5	6.0	8.5	μA	WDT ON(1), INH = open(1) V_{CT} = 0 V
WDT Discharge Current	Ictd	1.2	2.0	2.8	μA	WDT ON(1), INH = open(1) V_{CT} = 1.3 V
Watchdog Monitor Time Low	t_{WH}	3.0	5.0	7.0	ms	WDT ON(1), INH = open(1), C_{CT} = 0.01 μF (Ceramic Capacitor) (2)
Watchdog Reset Time	t_{WL}	1.0	1.7	2.4	ms	
CLK Input Pulse Width	t_{WCLK}	500	-	-	ns	
INH*						
WDT OFF Threshold Voltage	V_{HINH}	V_{OUT} × 0.8	-	V_{OUT}	V	
WDT ON Threshold Voltage	V_{LINH}	0	-	V_{OUT} × 0.3	V	INH is pulled down inside the IC when INH open.
INH Input current	I_{INH}	-	10	20	μA	V_{INH} = 5 V

(1) BD3021HFP only
(2) Characteristics of ceramic capacitor not considered.

Reference data

Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, V_{CLK} = GND

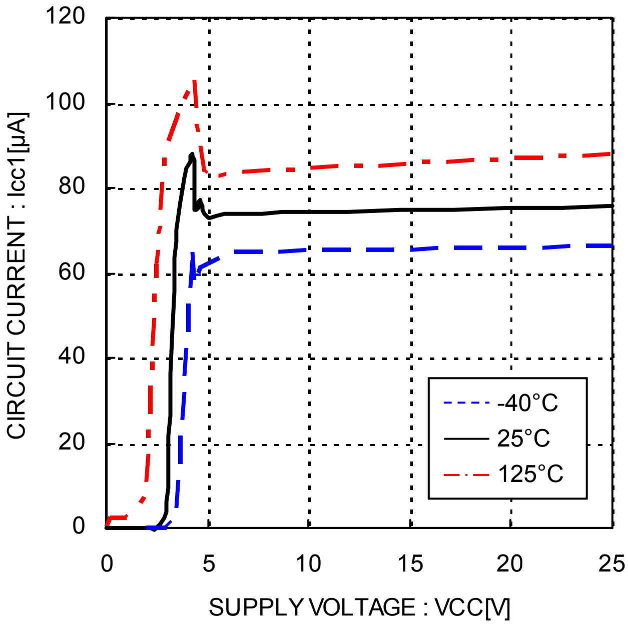


Figure 5. Circuit Current 1

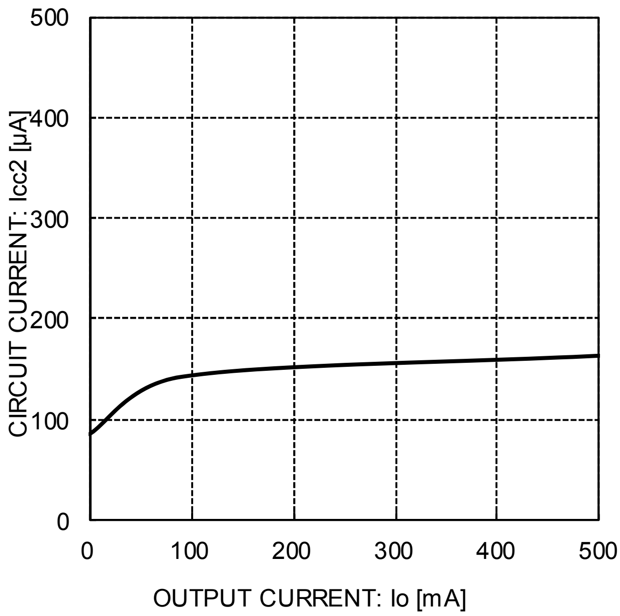


Figure 6. Circuit Current 2

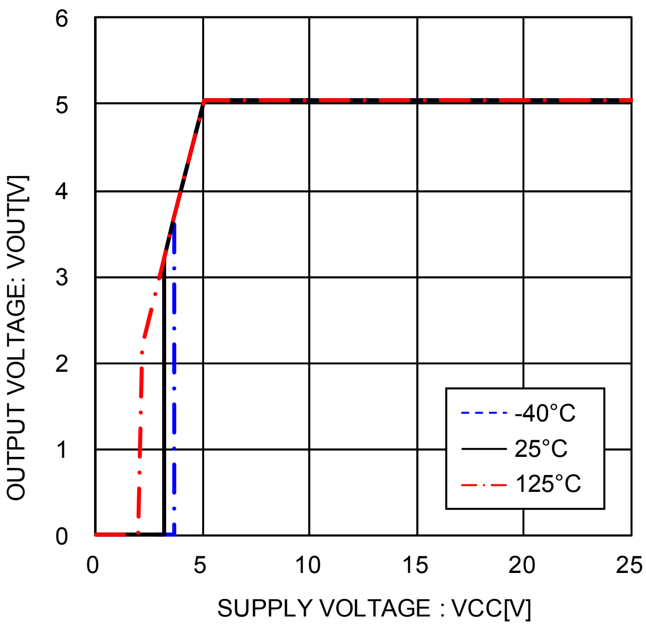


Figure 7. Input Stability

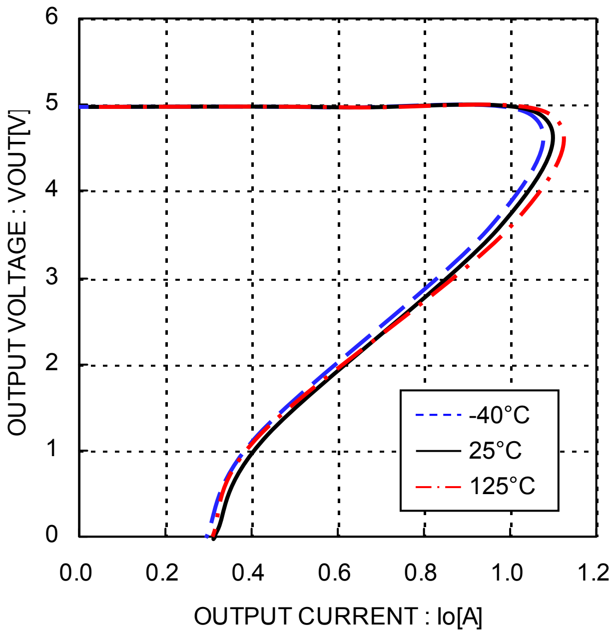


Figure 8. Lode Stability

Reference data

Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, V_{CLK} = GND

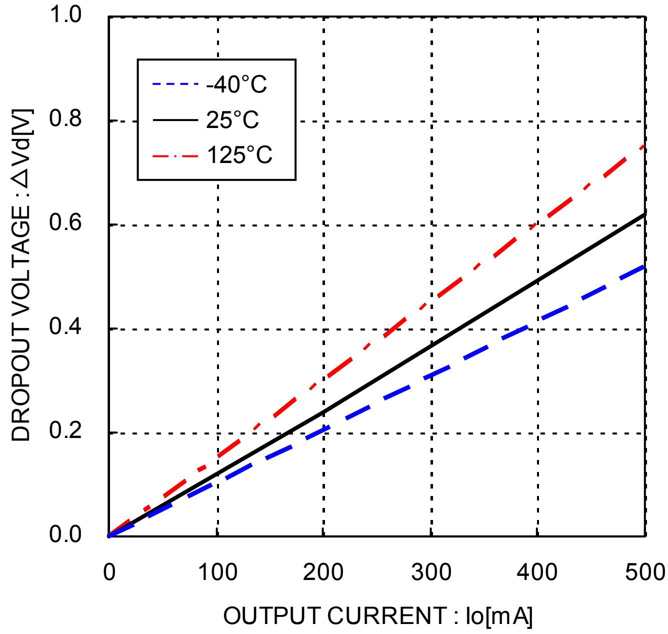


Figure 9. Dropout Voltage

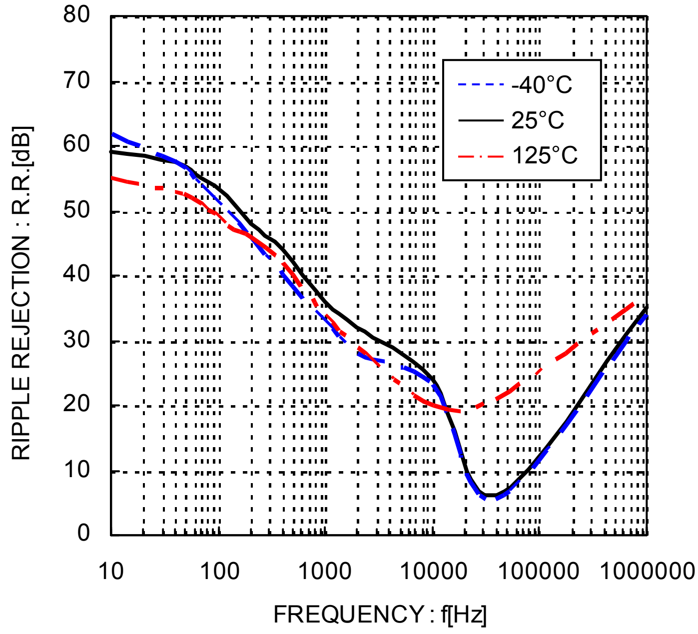


Figure 10. Ripple Rejection

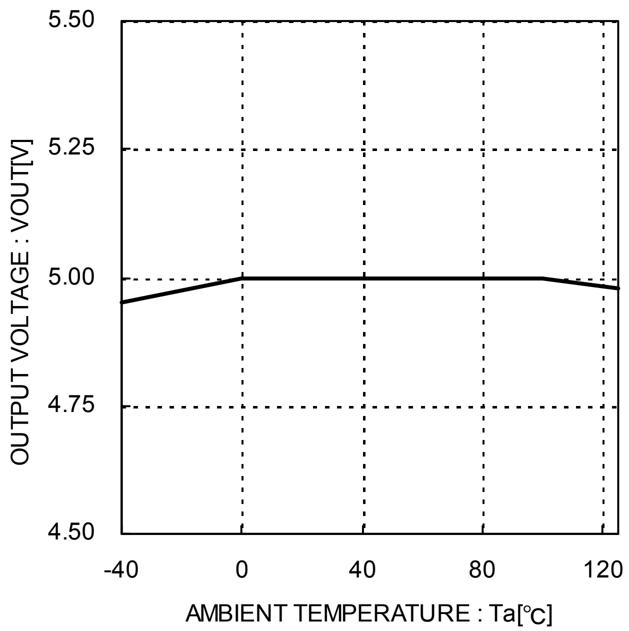


Figure 11. Output Voltage Temperature Characteristics

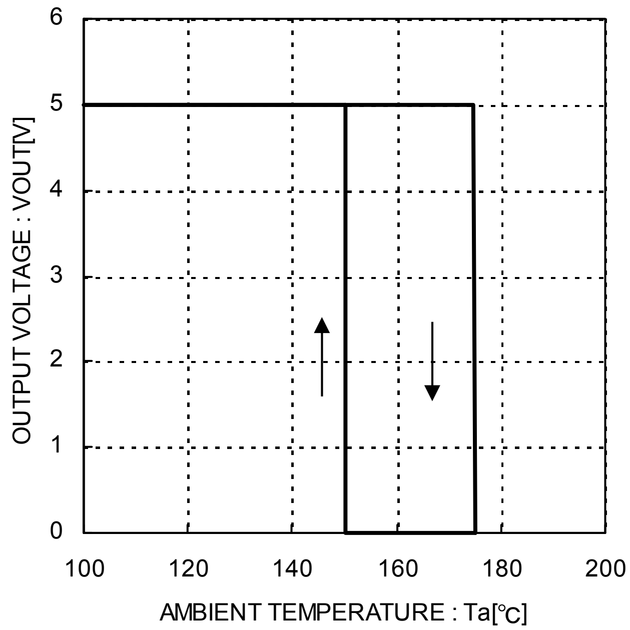


Figure 12. Thermal Shutdown Circuit Characteristics

Reference data

Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, V_{CLK} = GND

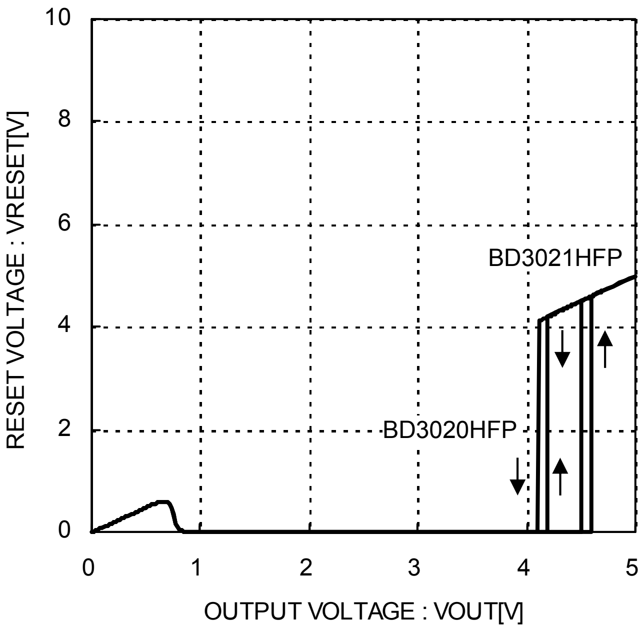


Figure 13. Detection Voltage (V_{CC}=V_{OUT})

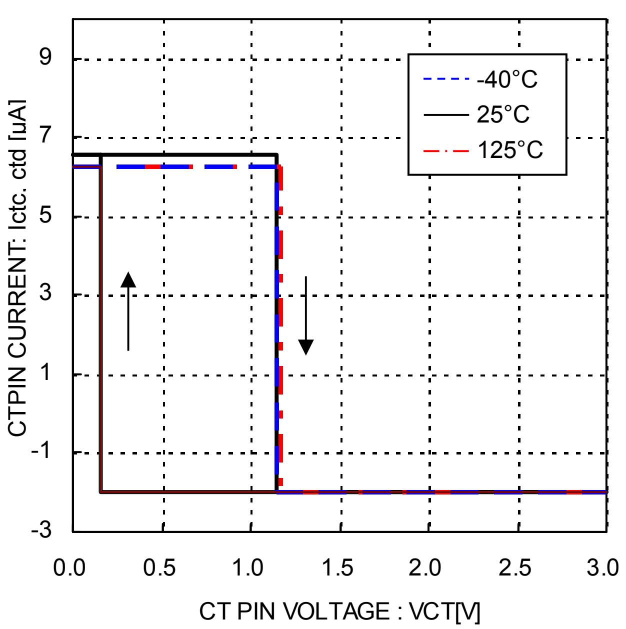


Figure 14. CT Pin Charge / Discharge Current (V_{CC}=5V)

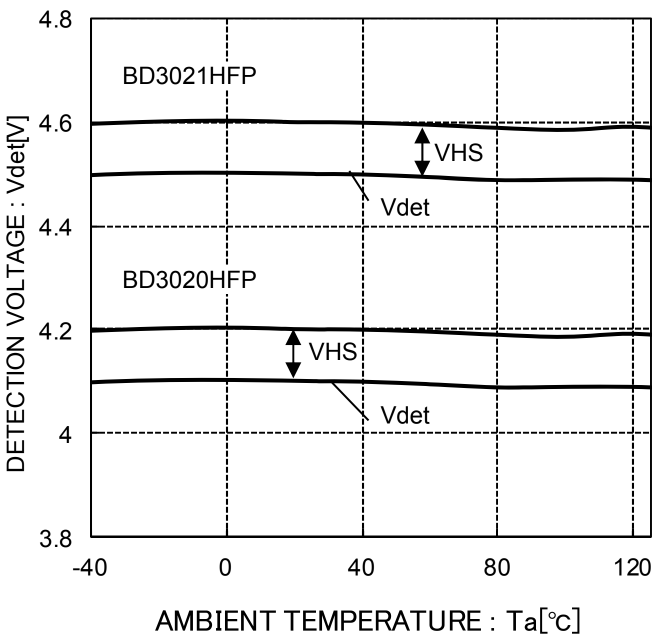


Figure 15. Reset Detection Voltage vs. Temperature

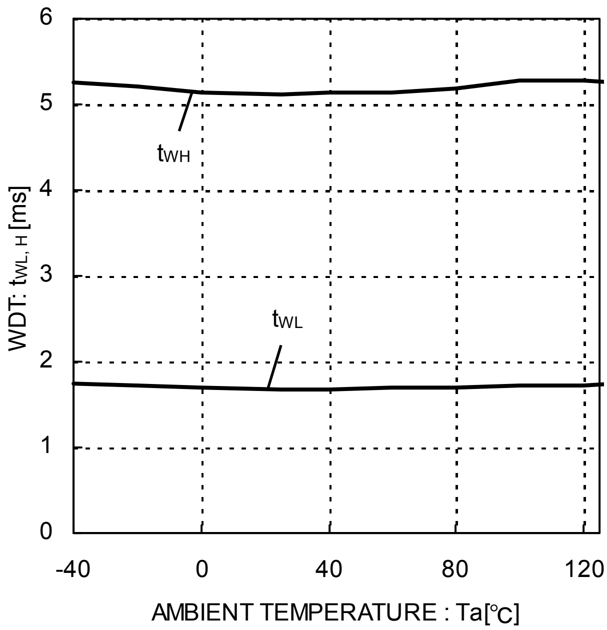
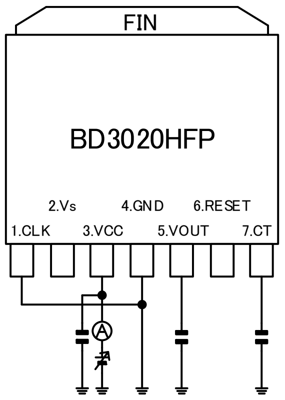
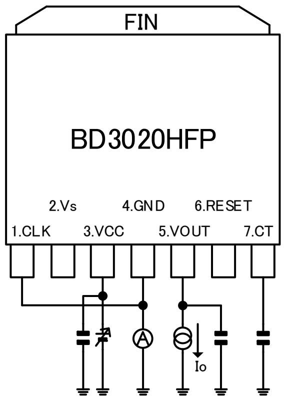


Figure 16. WDT Time vs. Temperature (C_{CT}=0.01μF)

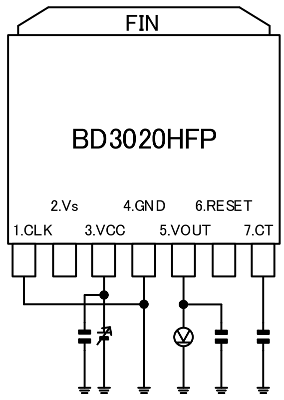
Measurement Circuits (BD3020HFP)



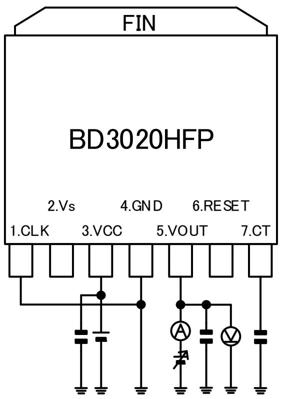
Measurement setup for Figure 5.



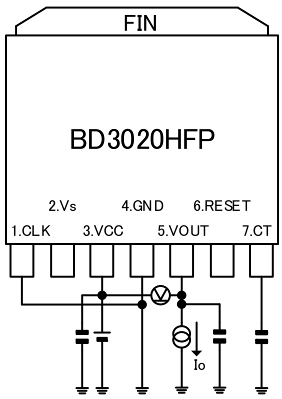
Measurement setup for Figure 6.



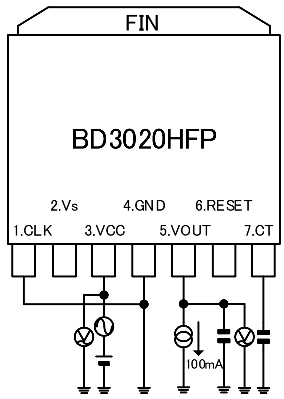
Measurement setup for Figure 7, 11, 12.



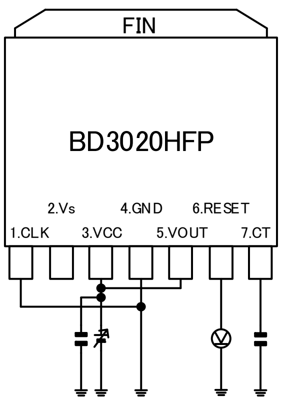
Measurement setup for Figure 8.



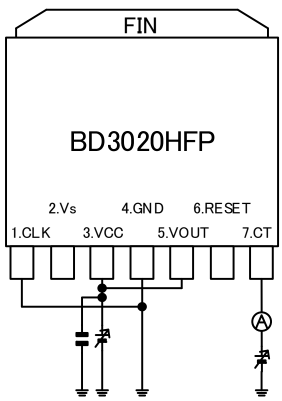
Measurement setup for Figure 9.



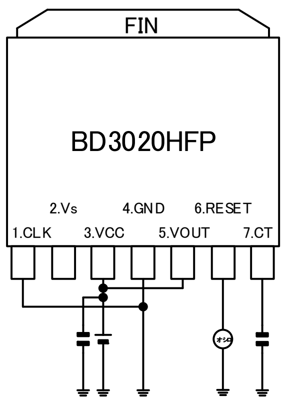
Measurement setup for Figure 10.



Measurement setup for Figure 13, 15.

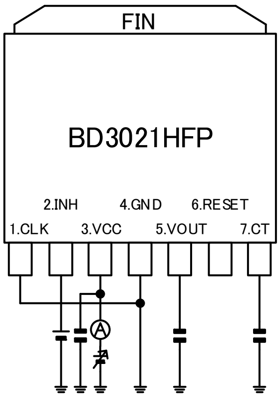


Measurement setup for Figure 14.

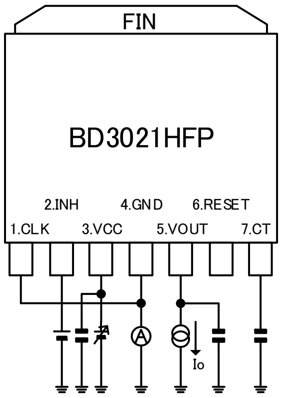


Measurement setup for Figure 16.

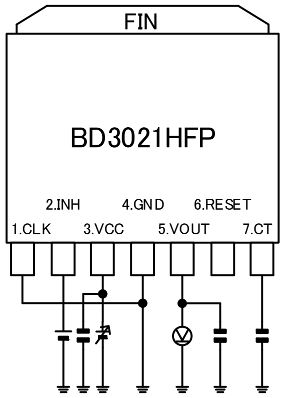
Measurement Circuits (BD3021HFP)



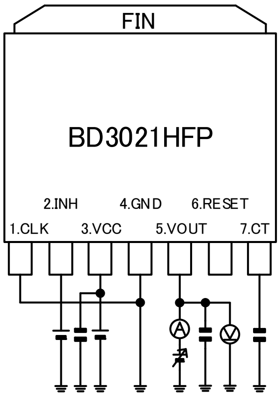
Measurement setup for Figure 5.



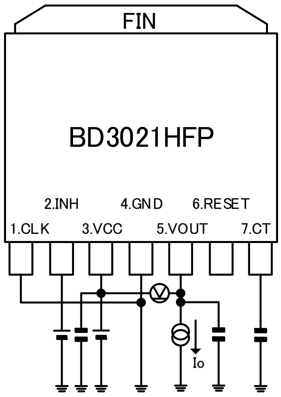
Measurement setup for Figure 6.



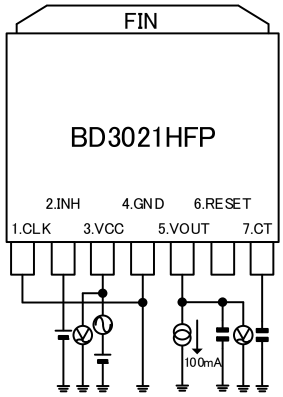
Measurement setup for Figure 7, 11, 12.



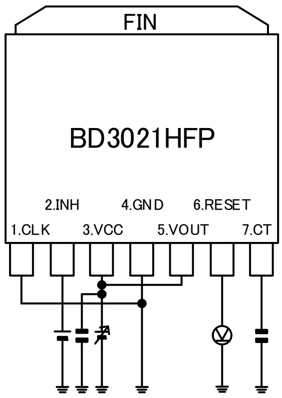
Measurement setup for Figure 8.



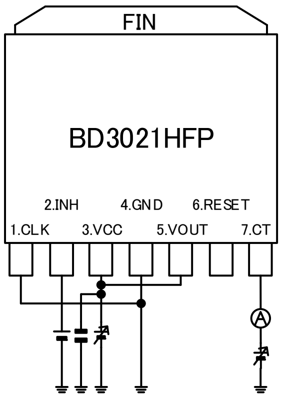
Measurement setup for Figure 9.



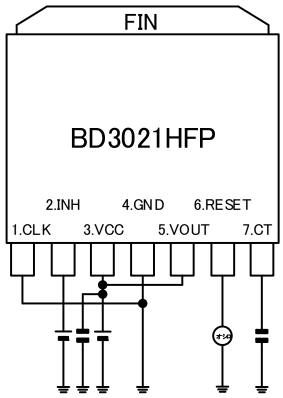
Measurement setup for Figure 10.



Measurement setup for Figure 13, 15.

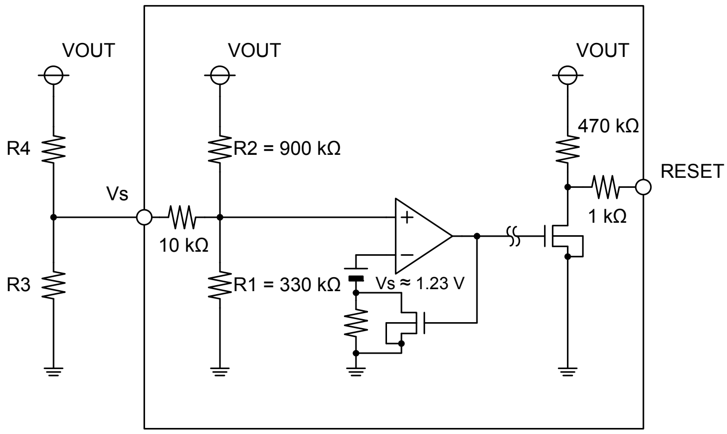


Measurement setup for Figure 14.



Measurement setup for Figure 16.

BD3020HFP Detection Voltage Adjustment (Resistance value is typical value)



IC Internal Block Diagram

When typical detection voltage is 4.1 V

$Vdet \approx Vs \times (R1 + R2) / R1$

- Vdet : Reset detection voltage
- Vs : Internal reference voltage (MOS input)
- R1, R2 : IC internal resistor
  (Voltage detection precision is tightened up to ±2 % by laser-trimming the R1 and R2)

Vs will fluctuate 1.23 V ±6.0 %.
The reset detection voltage can be adjusted by connecting resistors on the Vs terminal.
Insert pull down resistor R3 (lower resistance than R1) in between Vs-GND, and pull down resistor R4 (lower resistance than R2) in between Vs-VOUT to adjust the detection voltage.
By doing so, the detection voltage can be adjusted by the calculation below.

$$Vdet = Vs \times [\{R2 \times R4 / (R2 + R4)\} + \{R1 \times R3 / (R1 + R3)\}] / \{R1 \times R3 / (R1+R3)\}$$

When the output resistance value is as small enough to ignore the IC internal resistance, you can find the detection voltage by the calculation below.

$$Vdet \approx Vs \times (R3 + R4) / R3$$

Adjust the resistance value by application as the circuit current will increase due to the added resistor.

BD3020/21HFP Power on Reset / Watchdog Timer

Power ON reset (output delay time) is adjustable by CT pin capacitor.

t_{dLH} (S) ≈ (1.15 V × CT capacitance (μF)) / Ictc (μA) (Typ)

- t_{dLH} : Output delay time (power ON reset)
- 1.15 V : Upper switching threshold voltage (Typ)
- CT capacitance : Capacitor connected to CT pin
- Ictc : WDT charge current

Calculation example) with 0.01 μF CT pin capacitor

t_{dLH} (S) = 1.15 V × 0.01 μF / 6 μA

≈ 1.9 ms

*If the CT capacitance is not the same as the condition on the electrical characteristics table, i.e., 0.01 μF, choose the capacitance value in ratio referring to the above equation.

Watch Dog Timer (WDT t_{WH}, t_{WL}) is adjustable by the CT pin capacitor

t_{WH} (S) ≈ 1.00 V × CT capacitance (μF)) / Ictd(μA) (Typ)

t_{WL} (S) ≈ 1.00 V × CT capacitance (μF)) / Ictc(μA) (Typ)

- t_{WH} : Watchdog monitor time Low (delay time to turn the reset ON)
- t_{WL} : Watchdog reset time (time the reset is ON)
- 1.00 V : Upper switching threshold voltage - lower switching threshold voltage
- CT capacitance : CT pin capacitor *Shared with power ON reset
- Ictc : WDT charge current
- Ictd : WDT discharge current

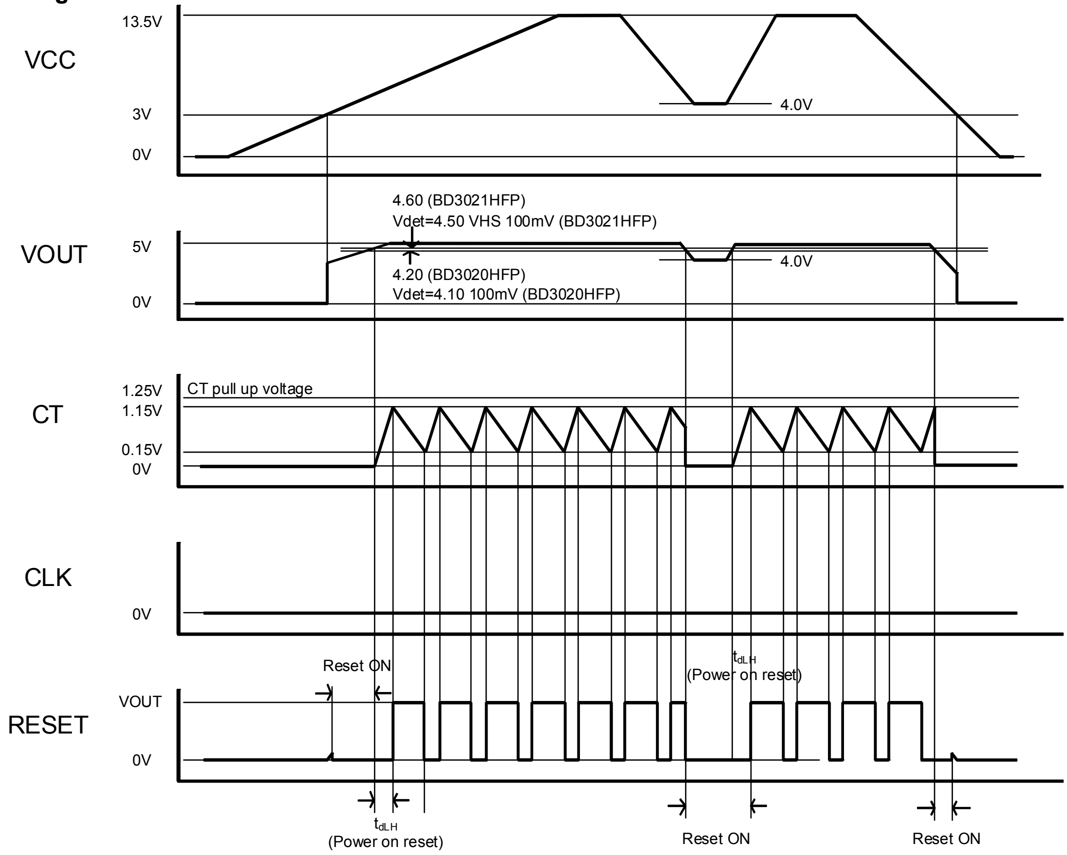
Calculation example) with 0.01 μF CT pin capacitor

t_{WH} (S) ≈ 1.00 V × 0.01 μF / 2 μA ≈ 5.0 ms (Typ)

t_{WL} (S) ≈ 1.00 V × 0.01 μF / 6 μA ≈ 1.7 ms (Typ)

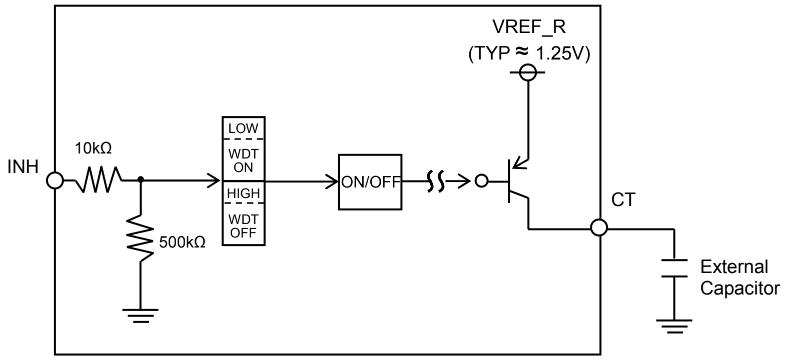
*If the CT capacitance is not the same as the condition on the electrical characteristics table, i.e., 0.01 μF, choose the capacitance value in ratio referring to the above equation.

<Timing Chart>



WDT timer ON / OFF switch INH (Resistance value is typical value)

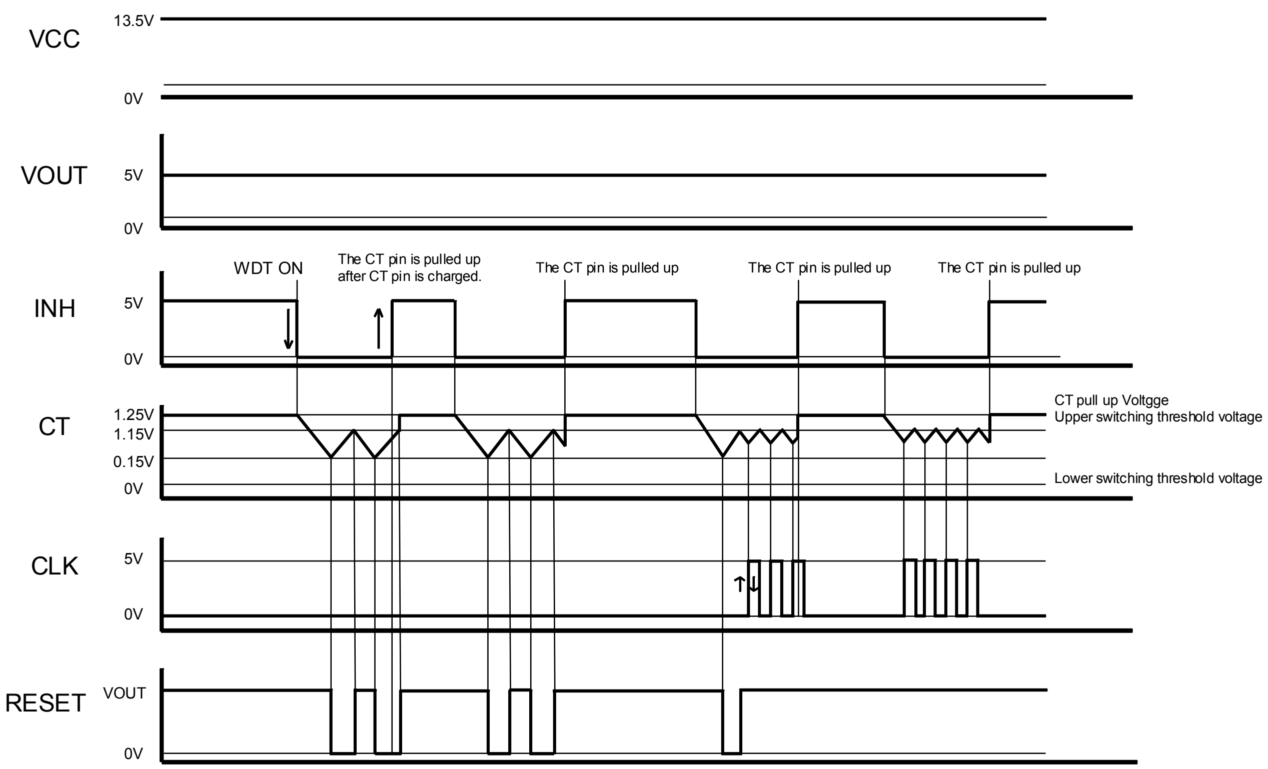
BD3021HFP has a switch INH to turn the WDT ON / OFF.



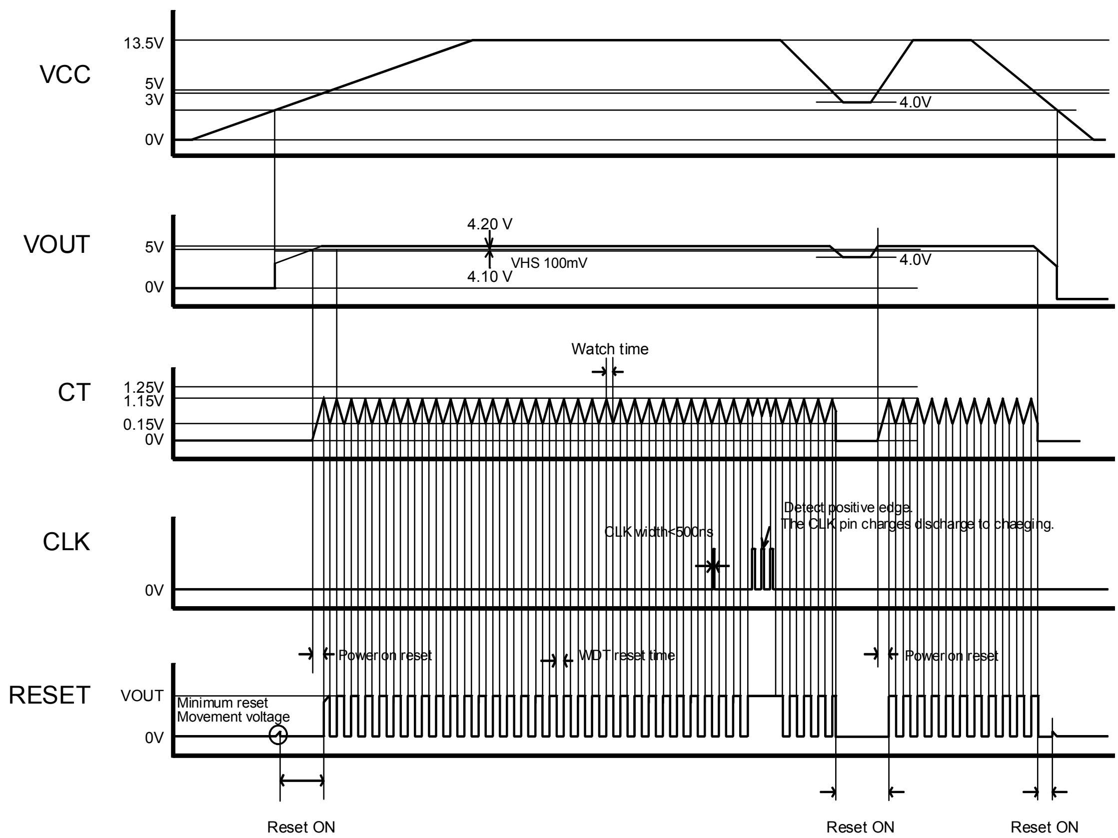
IC Internal Block Diagram

By using INH ON, CT potential can be pulled up to internal voltage VREF_R (invalid with power ON reset).

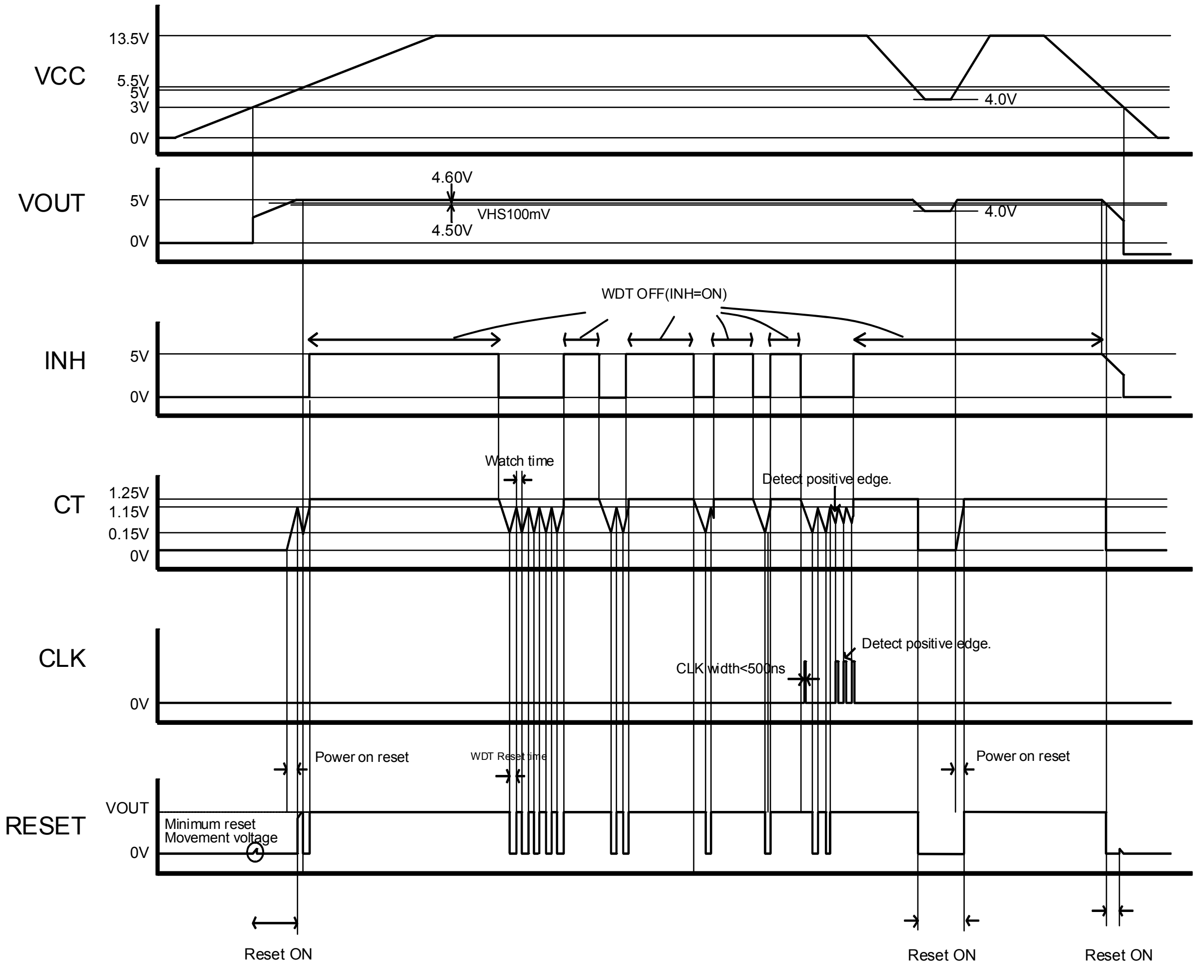
<Timing Chart> BD3021HFP



<Timing Chart> BD3020HFP



<Timing Chart> BD3021HFP

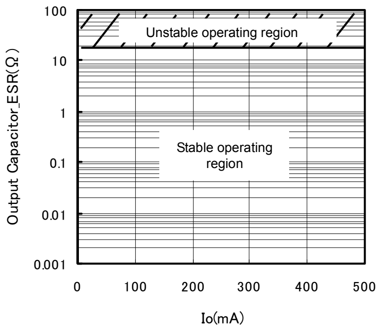


Pin Settings / Precautions

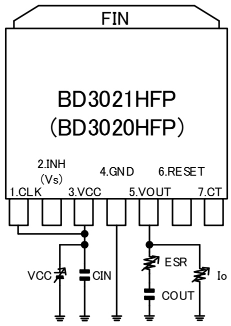
1. VCC Pin
   Insert a 0.33 μF to 1000 μF capacitor between the VCC and GND. The appropriate capacitance value varies by application. Be sure to allow a sufficient margin for input voltage levels.

2. Output pins
   In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND. We recommend using a capacitor with a capacitance of 0.1 μF to 1000 μF. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 0.1μF to 1000μF is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor refer to the Cout_ESR vs. Io data. The stable operation range given in the reference data is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.
   Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification.

V_{CC} = 5.6 V to 36 V
Ta = -40 °C to +125 °C Io = 0 A to 500 mA
C_{IN} = 0.33 μF to 100 μF, C_{OUT} = 0.1 μF to 100 μF



Output Capacitor_ESR vs Io (reference data)

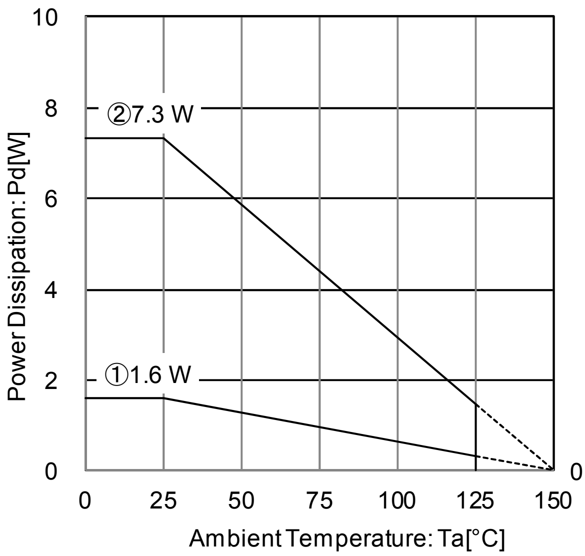


*Pin Settings / Precautions2 Measurement circuit

3. CT pin
   Connecting a capacitance of 0.01 μF to 1 μF on the CT pin is recommended.

Power Dissipation

■HRP7



IC mounted on ROHM standard board.
Board material: FR4
Board size: 70.0 mm × 70.0 mm × 1.6 mmt
(with thermal via on the board)
Mount condition: PCB and exposed pad are soldered.
Top copper foil: The footprint ROHM recommend.
+ wiring to measure.

①: 1-layer PCB
(Back surface copper foil area : 0mm × 0 mm)
②: 4-layer PCB
(Back surface copper foil area : 70.0mm × 70.0 mm)

Condition①: θja = 78.1 °C / W
Condition②: θja = 17.1 °C / W

Figure 17. Package Data
(HRP7)

Refer to Figure 17 thermal dissipation characteristics for usage above Ta = 25 °C. The IC's characteristics are affected heavily by the temperature, and if is exceeds its max junction temperature (Tjmax), the chip may degrade or destruct. Thermal design is critical in terms of avoiding Instantaneous destruction and reliability in long term usage.
The IC needs to be operated below its max junction temperature (Tjmax) to avoid thermal destruction. Refer to Figure 17 for HRP7 package thermal dissipation characteristics. Operate the IC within power dissipation (Pd) when using this IC.

Power consumption Pc (W) calculation will be as below

$$P_c = (V_{CC} - V_{OUT}) \times I_o + V_{CC} \times I_{CC}$$

Power dissipation Pd ≥ Pc

V_{CC} : Input Voltage
V_{OUT} : Output Voltage
Io : Load Current
Icc : Circuit Current

If load current Io is calculated to operate within power dissipation, it will be as below, where you can find the max load current I_{oMax} for the applied voltage V_{CC} of the thermal design.

$$I_o \le \frac{P_d - V_{CC} \times I_{CC}}{V_{CC} - V_{OUT}}$$

(Refer to Figure 6 for the Icc)

■Example) at Ta = 125 °C, V_{CC} = 12 V, V_{OUT} = 5 V

$$I_o \le \frac{1.452 - 12 \times I_{CC}}{12 - 5}$$

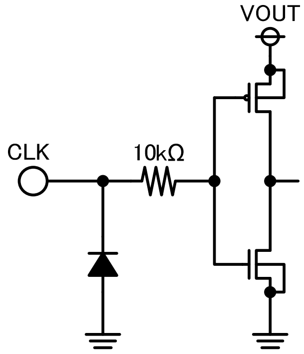
$$\left(\begin{array}{l}\theta ja = 17.1\ °C / W \rightarrow -58.4\ mV / °C \\ 25\ °C = 7.30\ W \rightarrow 125\ °C = 1.452\ W\end{array}\right)$$

Io ≤ 207 mA (Icc: 150 µA)

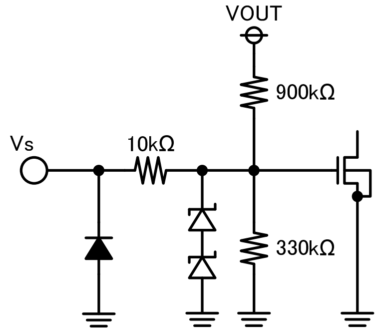
At Ta = 125 °C with Figure 17 ② condition, the calculation shows that ca 207 mA of output current is possible at 7 V potential difference across input and output.

I/O Equivalence Circuit (Resistance value is typical value)

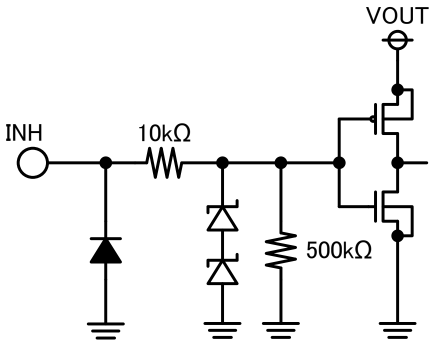
CLK (1pin)



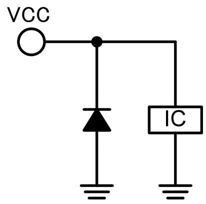
Vs (BD3020HFP 2pin)



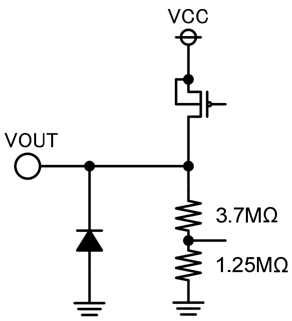
INH (BD3021HFP 2pin)



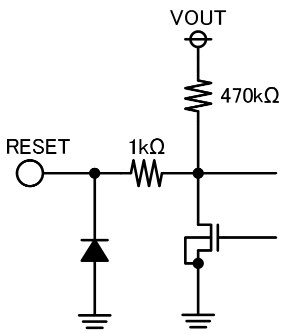
VCC (3pin)



VOUT (5pin)



RESET (6pin)



CT (7pin)

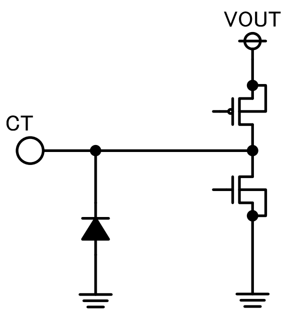


Figure 18. I / O equivalence circuit

Operational Notes

1. **Electrical characteristics**
Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

2. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

3. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

4. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

5. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

6. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

Use a thermal design that allows for a sufficient margin in light of the Pd in actual operating conditions.
Consider Pc that does not exceed Pd in actual operating conditions. ($Pd \geq Pc$)

(Tjmax: Maximum junction temperature = 150 °C, Ta: Peripheral temperature [°C],
θja: Thermal resistance of package-ambience [°C / W], Pd : Package Power dissipation [W],
Pc: Power dissipation [W], V_{CC}: Input Voltage, V_{OUT}: Output Voltage, Io: Load, I_{CC2}: Bias Current2)

Package Power dissipation : $Pd\ (W) = (Tjmax - Ta) / \theta ja$
Power dissipation : $Pc\ (W) = (V_{CC} - V_{OUT}) \times Io + V_{CC} \times I_{CC2}$

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

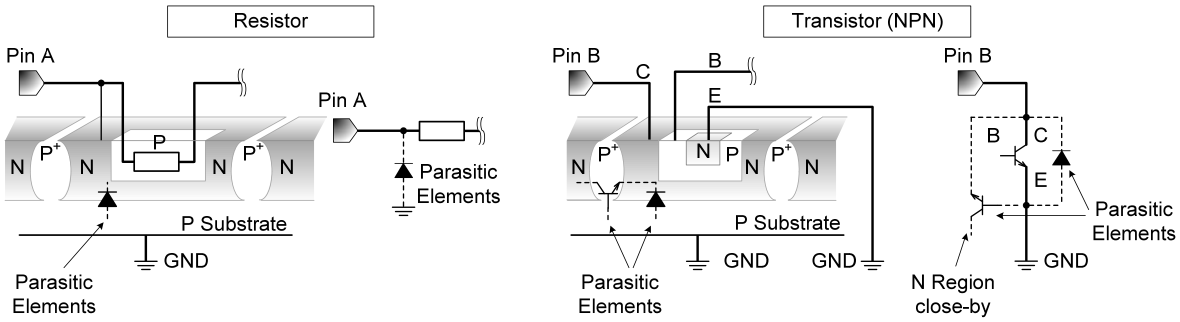


Figure 19. Example of monolithic IC structure

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Applications or inspection processes where the potential of the VCC pin or other pins may be reversed from their normal state may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000μF or lower in case VCC is shorted with the GND pin while the external capacitor is charged. Insert a diode in series with VCC to prevent reverse current flow, or insert bypass diodes between VCC and each pin.

15. Positive voltage surges on VCC pin

A power zener diode should be inserted between VCC and GND for protection against voltage surges of more than 50 V on the VCC pin.

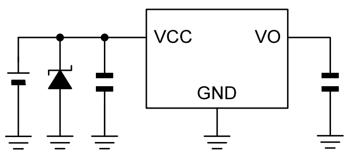


Figure 20. Application Examples 1

16. Negative voltage surges on VCC pin

A schottky barrier diode should be inserted between VCC and GND for protection against voltages lower than GND on the VCC pin.

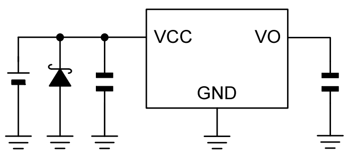


Figure 21. Application Examples 2

Operational Notes – continued

17. Output protection diode

Loads with large inductance components may cause reverse current flow during startup or shutdown. In such cases, a protection diode should be inserted on the output to protect the IC.

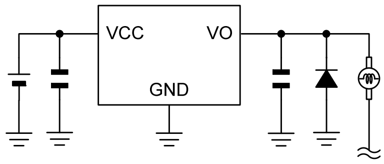
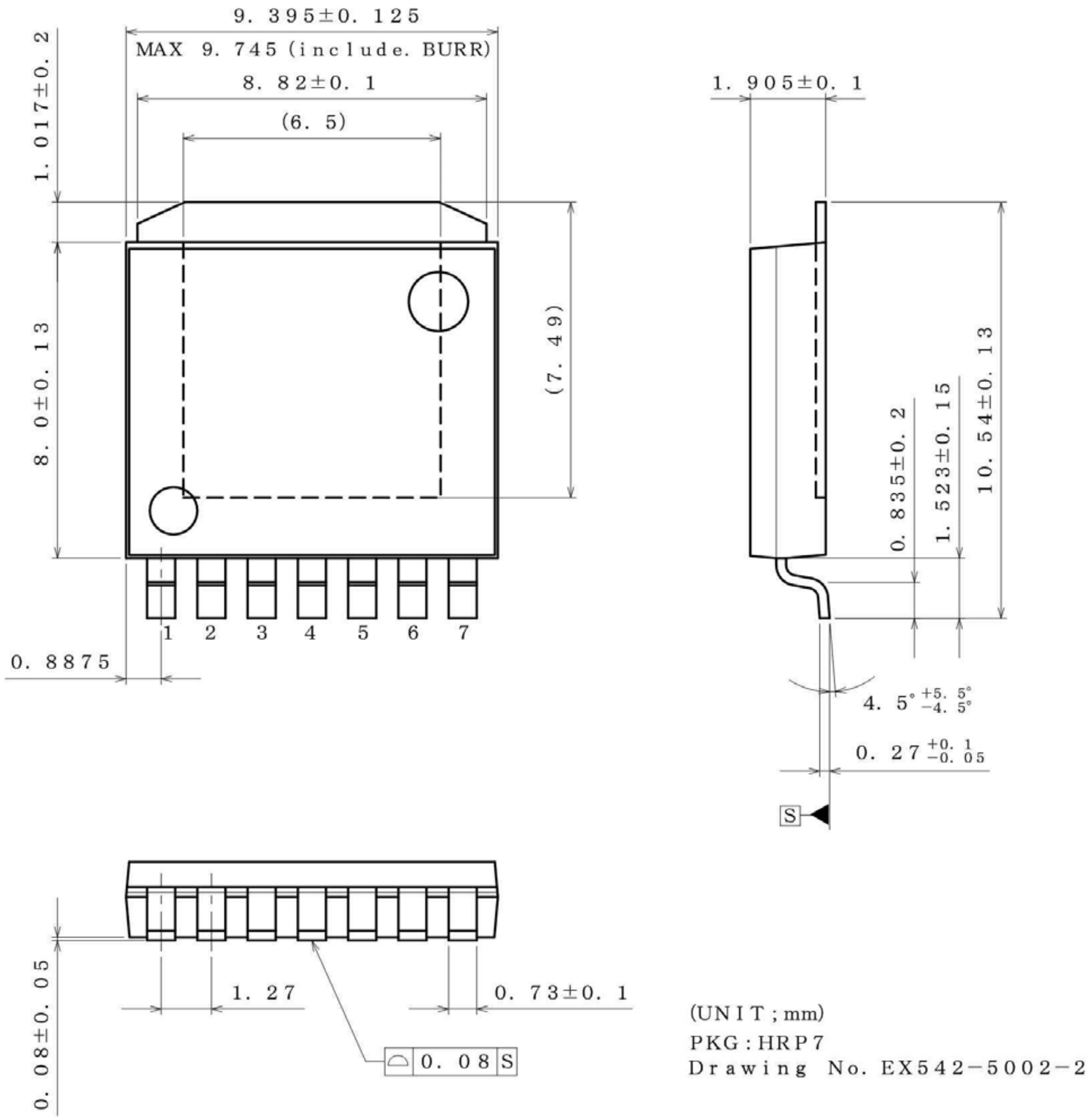


Figure 22. Application Examples 3

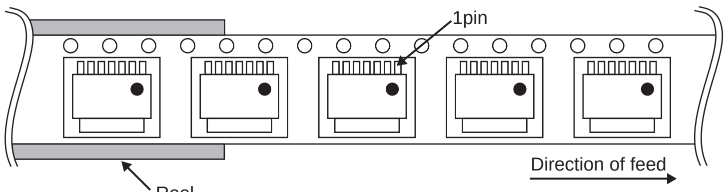
Physical Dimension, Tape and Reel Information

Package Name	HRP7



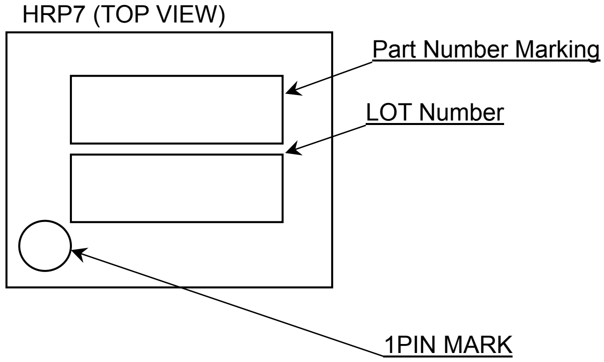
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagram



Product Name	Part Number Marking
BD3020HFP	BD3020
BD3021HFP	BD3021

Revision History

Date	Revision	Changes
10.Nov.2015	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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